

Key: IEEE JNL = IEEE Journal or Magazine, IEE JNL = IEE Journal or Magazine, IEEE CNF = IEEE Conference, IEE CNF = IEE Conference, IEEE STD = IEEE Standard

1. Regular realization of symmetric functions using reversible logic

Perkowski, M.; Kerntopf, P.; Buller, A.; Chrzanowska-Jeske, M.; Mishchenko, A.; Xiaoyu Song; Al-Rabadi, A.; Jezwiak, L.; Coppola, A.; Massey, B. Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on

2001 Page(s):245 - 252

IEEE CNF

2. A reversible evolvable Boolean network architecture and methodology to overcome the heat generation problem. In molecular scale brain building

de Garis, H.; Dinerstein, J.; Sriram, R.

Evolvable Hardware, 2002. Proceedings. NASA/DoD Conference on

2002 Page(s): 274 - 275

IEEE CNF

Reversible logic circuit synthesis

Shende, V.V.; Prasad, A.K.; Markov, I.L.; Hayes, J.P. Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on 10-14 Nov. 2002 Page(s): 353 - 360

IEEE CNF

Spectral and two-place decomposition techniques in reversible logic

Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on Volume 2, 4-7 Aug. 2002 Page(s): II-493 - II-496 vol.2

IEEE CNF

Synthesis of reversible logic circuits

Shende, V.V.; Prasad, A.K.; Markov, I.L.; Hayes, J.P. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 22, Issue 6, June 2003 Page(s): 710 - 722

IEEE JNL

6. Evolved reversible cascades realized on the CAM-brain machine

Buller, A.; Perkowski, M. Evolvable Hardware, 2003. Proceedings. NASA/DoD Conference on 9-11 July 2003 Page(s): 246 - 251

IEEE CNF

7. A transformation based algorithm for reversible logic synthesis

Miller, D.M.; Maslov, D.; Dueck, G.W. Design Automation Conference, 2003. Proceedings 2-6 June 2003 Page(s): 318 - 323

IEEE CNF

8. Transformation-based synthesis of networks of Toffoli/Fredkin gates

Dueck, G.W.; Maslov, D.; Miller, D.M. Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on Volume 1, 4-7 May 2003 Page(s): 211 - 214 vol.1

IEEE CNF

Reversible logic synthesis for minimization of full-adder circuit

Hafiz Md Hasan Babu; Md Rafigul Islam; Ahsan Raja Chowdhury; Syed Mostahed Ali Chowdhury Digital System Design, 2003. Proceedings. Euromicro Symposium on 1-6 Sept. 2003 Page(s): 50 - 54

IEEE CNF

10. Fredkin/Toffoli templates for reversible logic synthesis

Maslov, D.; Dueck, G.W.; Miller, D.M.

Computer Aided Design, 2003. ICCAD-2003. International Conference on

9-13 Nov. 2003 Page(s): 256 - 261

IEEE CNF

11. Synthesis of full-adder circuit using reversible logic

Babu, H.M.H.; Islam, M.R.; Chowdhury, S.M.A.; Chowdhury, A.R. VLSI Design, 2004. Proceedings. 17th International Conference on 2004 Page(s): 757 - 760

IEEE CNF

12. Synthesis of reversible logic

Agrawal, A.; Jha, N.K.

Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings

Volume 2, 16-20 Feb. 2004 Page(s): 1384 - 1385 Vol.2

IEEE CNF



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	Туре	L#	Hits	Search Text	DBs
1	BRS	L3	200	turing adj machine	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L4	95	3 and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L2	71	reversible adj logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L5	188	(2 3 4) and input and output	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
5	BRS	L6	166	5 and control	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L7	393	morita-\$.in. and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L8	1249	lee-j\$.in. and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L9	5	8 and reversible	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
9	BRS	L10	2	7 and reversible	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB